

THE PHASE AMPLITUDE CONTROLLED BIT STREAM ADDER

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This research introduces a one-bit signal processing structure called the phase amplitude control bit stream adder. The proposed method is a digital filter structure, which is capable of controlling amplitude and phase over a one-bit sine wave without the need of directly multiplying the one-bit stream with a floating-point constant. The method allows performing signal processing in the one-bit domain, thus maintaining high-resolution characteristics associated with one-bit signals. It has applications in precision variable oscillator control and in oscillator bank additive synthesis reconstruction models. The research also explores a method for one-bit oscillator bank synthesis, without using intermediate multi-bit stages directly applied to the signal.

INTRODUCTION

Oversampled one-bit sigma delta modulated (SDM) signals enable us to get rid of decimation filters and steep low pass filters (LPF) [1], which compromise the phase response of digital signals, making them ideal for high-resolution audio applications. They have excellent impulse and transient response. Also they are highly tolerant to bit errors during transmission, compared to standard multi-bit Nyquist sampled pulse code modulated signals [2]. In an attempt to preserve these characteristics, signal processing applied directly to the one-bit stream without multiple multi-bit stages is desirable. In the following sections a one-bit signal processing method, which aims to reduce multi-bit stages, is presented.

Much research has been done in one-bit signal processing in the past years in hope of developing sufficient tools for one-bit audio, possibly as a result of solving some of the signal processing constraints resulting from the introduction of the Super Audio Compact Disc (SACD) format. An excellent introduction to this topic can be found in [1].

One-bit SDMs are currently used as a building block to one-bit signal processing. A common practice is to use SDMs together with Low Pass Filters (LPF) to change from one-bit to multi-bit and backwards. This is to apply more traditional Pulse Code Modulated (PCM) processing techniques to one-bit signals [3]. SDM have also find an important place in Analogue to Digital (ADC) and Digital to Analogue Converters (DAC). Unfortunately SDM are susceptible of introducing errors [4, 5]. Therefore, the more multi-bit stages used during the one-bit signal processing the more the

original signal integrity is jeopardize. For this reason one-bit signal processing with no intermediate multi-bit stages is desirable for high-resolution applications. Currently efforts in one-bit signal processing are focus on SDM improvement, but in the authors' knowledge, few of them, e.g. [6], are concerned with directly processing one-bit signals while minimising multi-bit processing stages.

Ideally, signal processing of the one-bit stream should retain high order noise shaping while not having intermediate multi-bit stages. This remains unsolved, even for the most basic operations like addition and multiplication. In the case of direct multiplication of two one-bit SDM signals, the individual noise shaping characteristics of signals are lost due to the convolution of the error terms involved in this process, and will result in multi-bit streams. Another related unsolved problem is the addition of two one-bit SDM signals without incurring any gain loss. The method proposed herein will use an averaging method for performing addition. This will be explained in more detail in the following section.

1 THE BSA

The development of this method is widely based on the Bit Stream Adder (BSA) in [7]. In this work P. O'leary and F. Maloberti describe a method of adding one-bit over sampled data streams. The method they propose works in a similar manner to a first order SDM and its operation is valid only for low frequencies (with respect to the over sampled sampling frequency).

During the development of the PACBSA it was found that the BSA proposed in [7] performs more like an averaging device and not like a full adder. This means it has a 6dB overall gain loss compared to a standard multi-bit addition. These results are in agreement with [8]. This means that a division by two term should be incorporated into the BSA mathematical description in order to reflect the 6dB loss. This is equivalent to an averaging device rather than an adding device. Therefore the output of the BSA for low frequencies should be expressed as:

$$Y(z) = \frac{X_1(z) + X_2(z)}{2} \quad (1)$$

Where $Y(z)$ is the one-bit average output and $X_1(z)$ and $X_2(z)$ represent the one-bit stream inputs to be averaged.

2 THE PACBSA

The Phase Amplitude Controlled Bit Stream Adder (PACBSA) is a digital filter structure, which is capable of controlling the amplitude and phase of a one-bit sine wave without the need to use intermediate multi-bit stages. THE PACBSA is based on the BSA averaging structure in [7]. The control of phase and amplitude is handled by a multi-bit word, which relates to the one-bit output of the PACBSA.

The method works by adding previously synthesized one-bit sine waves, whose relative phase has been manipulated in order to achieve a desired phase and amplitude output when adding them. Because the addition of the one-bit sine waves is done using a BSA, individual sinusoidal components with specified amplitude and phase can be synthesised without the need for multi-bit operations applied to the one-bit signal. At a later stage, all synthesis sinusoid components can be added to reconstruct a complex wave.

The proposed method has a fixed number of amplitude output levels, whose resolution and quantity is in proportion to the sampling rate. This implies that the higher the sampling rate, the better amplitude resolution. It also means that the method is frequency dependant and will be more accurate for low frequencies. This makes the method suitable for highly over sampled signals.

The PACBSA uses the fact that a target phasor of a known frequency is to be output. This is typical of an additive synthesis signal reconstruction method where all the target output phasors are previously known. For an input sinusoid $X(n)$, whose frequency corresponds to the frequency of a desired target phasor, the following

PACBSA general diagram is presented.

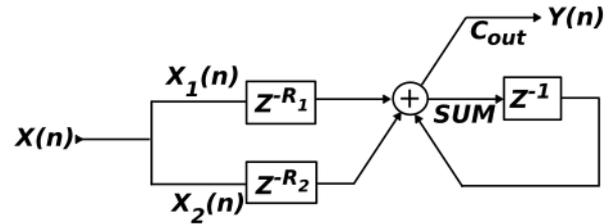


Figure 1. PACBSA General structure

Given that the output of the PACBSA, $Y(n)$, is a phasor of the form $Y \angle \phi$, the magnitude is given by:

$$Y = 10 \log(2 * (1 + \cos \alpha)) - 6 + X_{max} \quad (2)$$

where X_{max} is the maximum magnitude of the one-bit sine wave input, whose amplitude and frequency (fm) is determined by the system designer. The X_{max} should be the maximum encodable amplitude possible so that the dynamic range gets maximised. On the other hand, fm should be in accordance to the target phasor frequency to be synthesised. The -6 constant corresponds to the compensation of the averaging effect of the BSA contained inside the PACBSA structure. It is worth mentioning that even though a 6dB gain loss is expected due to the use of a BSA, the PACBSA is capable of achieving unity gain levels. This also means that the PACBSA maximum amplitude output is limited by the magnitude of $X_{max}(n)$.

α is a multi-bit word that corresponds to the control angle of the PACBSA and it is responsible for controlling the amplitude magnitude of the output phasor. α is the relative phase difference between $X_1(n)$ and $X_2(n)$ after the delay stage is applied to them. When implementing the PACBSA, α should be a number such that when $\alpha/2$ is calculated it corresponds to an integer sample of fm , where fm is the sinusoidal frequency to be synthesised. The control angle is given by the following equation:

$$\alpha_{samples} = \frac{\left(\frac{fs}{fm} \right) \left(a \cos \left[\left(\frac{10^{\left(\frac{Y+6-X_{max}}{10} \right)}}{2} \right) - 1 \right] \right)}{360} \quad (3)$$

Where fs represents the over sampled frequency and fm represent the frequency of the target phasor to be outputted.

Finally the delay needed to be applied to $X_1(n)$ and $X_2(n)$ in order to control the amplitude and phase of the output sine wave is:

$$R_1 = +\alpha / 2_{samples} + \phi_{samples} \quad (4)$$

$$R_2 = -\alpha / 2_{samples} + \phi_{samples} \quad (5)$$

A simplified filter can be derived from Figure 1 if the phase of $X(n)$, which is a one-bit sine wave, is known and can be determined at all times. This is a reasonable assumption, especially for pre-buffered indexed sinusoids. Figure 2 shows the simplified PACBSA structure.

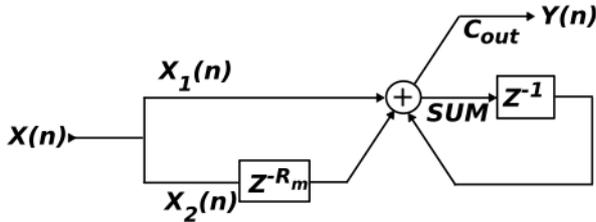


Figure 2. Single delay line PACBSA

Given the phase knowledge of $X(n)$, the absolute phase at which $X(n)$ starts is given by

$$R_s = +\alpha / 2_{samples} + \phi_{samples} \quad (6)$$

The value of the delay needed to be applied to $X_2(n)$ is:

$$R_m = -\alpha_{samples} + \phi_{samples} \quad (7)$$

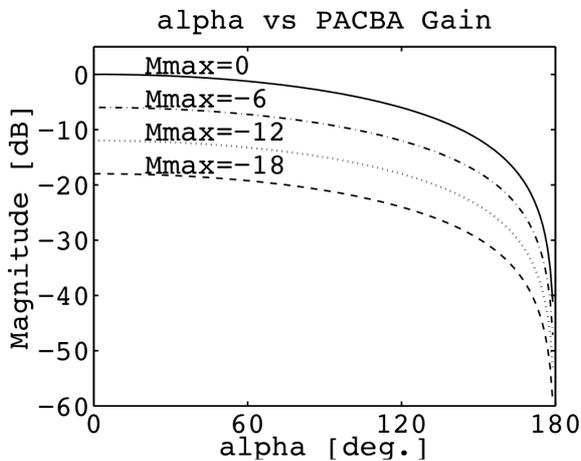


Figure 3. Amplitude Vs Control angle of a PACBSA for different X_{max}

In figure 3 the characteristic gain as a function of the PACBSA control angle α is presented. It can be seen that the characteristic curve is smoother at high levels and decays with a higher slope as the control angle increments. This can prove useful for cross-fading of signals. Also it can be seen that by using different X_{max} , the dynamic range limits of the system are set. The

higher the magnitude of X_{max} , the higher the dynamic range of the system.

2.1 The Additive PACBSA

The PACBSA makes absolutely no change to the bit stream if both one-bit streams being added are the same. So for two bit streams with same absolute phase, no noise is introduced by the PACBSA. The moment two equal bit streams have nonzero relative phase, first order noise is to be expected. This also applies to standard additive BSA.

Figure 4 shows the results for simulations of an additive PACBSA, based on figure 1, achieving a signal to noise ratio (SNR) of up to 142dB for an α of one. This was within a bandwidth from 10 Hz to 22.05 kHz with a 6th order SDM input sinusoid sampled at 44100*320 Hz. Schreir's Delta Sigma Toolbox was used for generating the test signals [9]. More information on the tool box can be found in [10]. Notice in Figure 4 how the SNR characteristics of the input signal remain unchanged for a 0° angle.

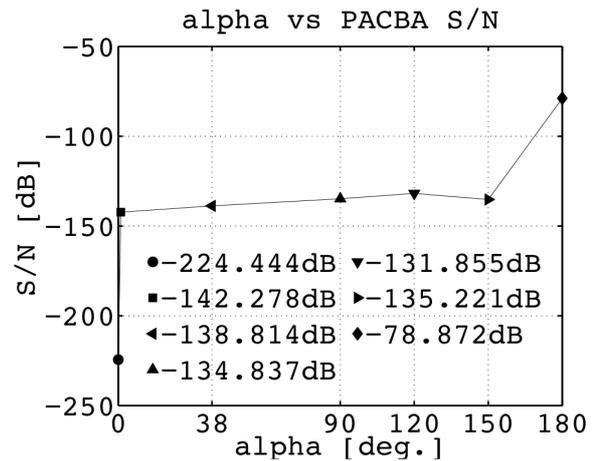


Figure 4. Control angle of an additive PACBSA vs SNR

2.2 The Subtractive PACBSA

If the bit stream $X_2(n)$ is inverted while $X_1(n)$ remains un-inverted a subtractive PACBSA can be implemented. In this case an extra 180° constant is to be added to Equations 5 and 7 to compensate for the polarity inversion of $X_2(n)$. The performance of the subtractive system is equivalent to the results shown for the additive PACBSA, except for the fact that when both $X_2(n)$ and $X_1(n)$ are in phase, first order noise will still be present. This is due to the fact that both streams are not exactly the same. If the extra 180° term in equations 5 and 7 is replaced by 0° a total cancellation, over the whole bandwidth, due to direct polarity inversion of the bit stream will occur.

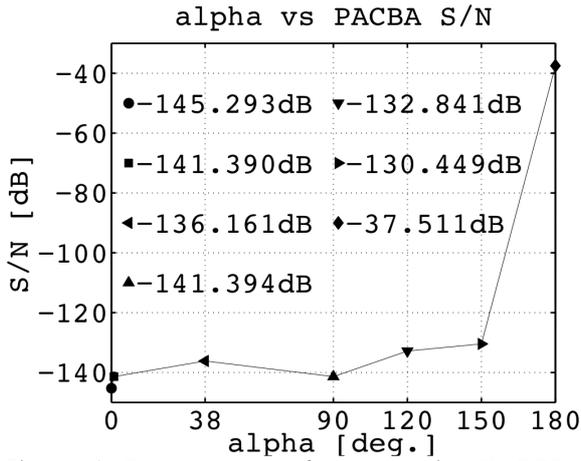


Figure 5. Control angle of a subtractive PACBSA v SNR

Figure 5 is an equivalent SNR plot to Figure 4 except here the input signal contains first order noise even for a control angle of 0° . The result of a total cancellation over the whole bandwidth, due to bit stream inversion, is also presented.

3 OVERSAMPLED OSCILLATOR BANK USING PACBSA

A method for using the BSA as a summing bus is presented in [8] as part of a delay based effect. If we apply the BSA summing bus to a PACBSA oscillator bank we can achieve a complex wave synthesis. If this method is used while manipulating the target phasor before synthesis, multiple signal processing operations like filtering, spectral and phase manipulation can be performed. A diagram of a general PACBSA oscillator bank showing target magnitude manipulation is shown in Figure 6.

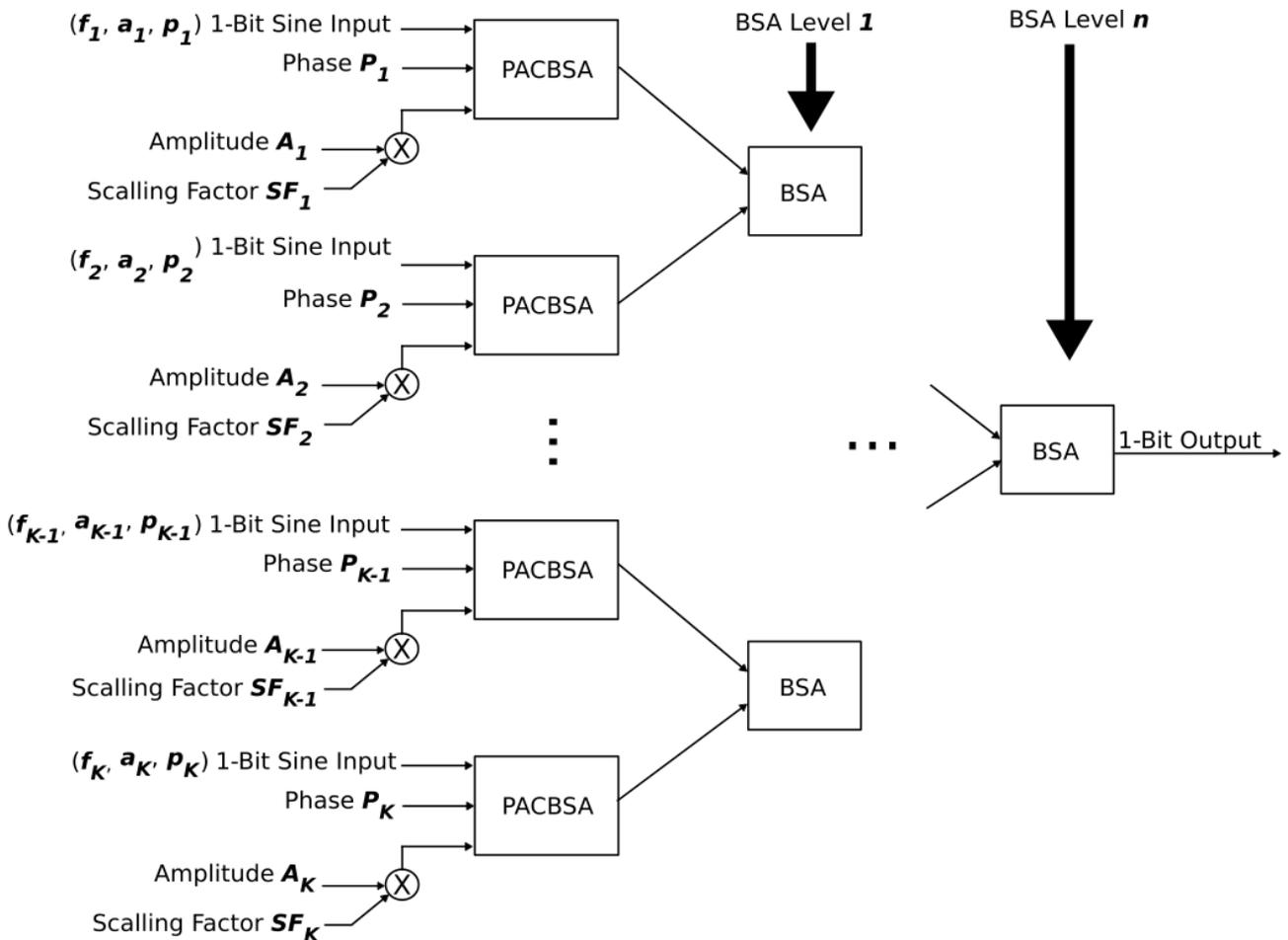


Figure 6. PACBSA structure for a one-bit oscillator bank synthesized with no multi-bit stages, for amplitude manipulation.

Based on this diagram it was found that for every level of BSA added to the summing bus, a 6dB reduction in the output level is present. Therefore the dynamic range is reduced as the number of sinusoidal components to be added is increased.

A complex signal conformed of sinusoids was synthesised using the PACBSA oscillator bank architecture shown in Figure 6. The system achieved a +/-0.01dB coding accuracy and an SNR of 113dB. The resulting plot is presented in Figure 7. The phasors and sampling rate used to synthesize the complex wave shown in Figure 6 are as follows:

$F_s=44100*320\text{Hz}$; $f_{m1}=30\text{Hz}@-28.52\angle 160^\circ$;
 $f_{m2}=700\text{Hz} @ -58.06\text{dB}\angle 20^\circ$; $f_{m3}=4000\text{Hz}@-38.06\text{dB}\angle 100^\circ$; $f_{m4}=15000\text{Hz}@-32.04\text{dB}\angle 70^\circ$.

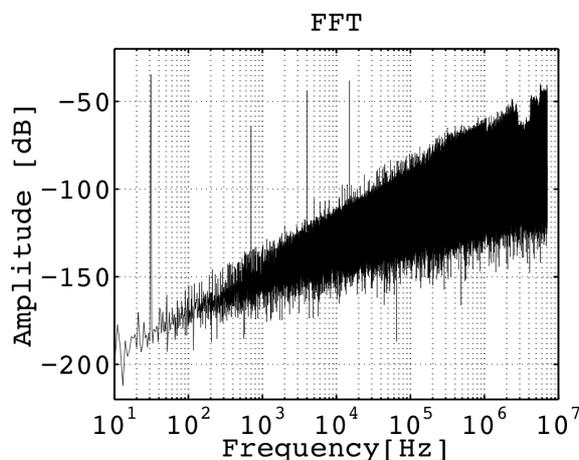


Figure 7. FFT of a Complex one bit sine wave with target phasor produced by the PACBSA oscillator bank of Figure 6. At the appendix.

Although the synthesis was accurate it is worth mentioning the following observations. The algorithm introduces first order noise due to the use of the BSA. This is because being an additive synthesis, the first order noise amplitude will increase proportionally with the complexity of the synthesis. Finally a scaling factor (SF) of 12dB was used to compensate for the gain loss introduced during the summing buss stage of the synthesis algorithm. Although compensation in the PACBSA stage is not a problem, this means that in the summing buss stage the dynamic range of the algorithms will be reduced in proportion to the number of summing buss levels in the algorithm.

4 CONCLUSIONS

A one-bit signal processing structure called the Phase Amplitude Controlled Bit Stream Adder (PACBSA) has been introduced. The structure manipulates the amplitude and phase of a one-bit sine wave without the

need to use intermediate multi-bit stages directly applied to the signal. The theory describing the PACBSA has been stated and proven to be accurate. A one-bit complex signal was synthesized without intermediate multi-bit stages. It was found that for a BSA buss a 6dB loss is expected for every level of iteration, this is also true for a single BSA. The proposed method performance improves with higher sampling rates.

In this research a method for synthesis and signal processing is proposed as a proof of concept that it is theoretically possible to achieve a one-bit signal processing without multi-bit stages, but achieving this while retaining an acceptable degree of noise shaping and a suitable dynamic range remains a subject of future study.

ACKNOWLEDGMENTS

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