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Exploiting Chaos in Multibit Sigma Delta Modulation

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Abstract- **When sigma-delta modulation is used for audio signal processing, limit cycles in the output may result in idle tones that are audible to the listener. We show that a multibit implementation of a modified first order sigma-delta modulator may be used to produce an effective, stable chaotic modulator that accurately encodes the input and helps remove the presence of idle tones.**

Introduction

Sigma delta modulation (SDM) is a popular method for high-resolution A/D and D/A conversion. It is frequently used in audio processing and has a wide range of applications. Sigma-delta modulators operate using a tradeoff between oversampling and low resolution quantization. A signal is sampled at higher than the Nyquist frequency, typically with one bit quantization, so that the signal may be effectively quantized with resolution on the order of 14-20 bits.[1] Recent work has concentrated on tone suppression[2-3], multibit[4] and chaotic SDM.[5]

The simplest sigma delta modulator consists of a 1-bit quantizer embedded in a negative feedback loop which also contains a discrete-time integrator, as depicted in Figure 1(a). The analog input to the modulator is oversampled and converted into a binary output. The system may be represented by the map[6]

$$U_n = \alpha U_{n-1} + X_{n-1} - Q(U_{n-1}) \qquad (1)$$

where X represents the analog input signal and Q is the quantizer

$$Q(u) = \begin{cases} 1 & \text{if } u \geq 0 \\ -1 & \text{if } u < 0 \end{cases} \qquad (2)$$

$Q(U_n)$ represents the quantization of input X_{n-1}. If $\alpha=1$, then this quantizes the difference between the input and the accumulated error. When the error grows sufficiently large, the quantizer will flip in order to reduce the error. On average, the quantization should equal to the input. Typically, the integrator leaks due to finite operational amplifier gain, which is represented by $\alpha<1$. If $\alpha>1$, then the modulator may behave chaotically for constant input.

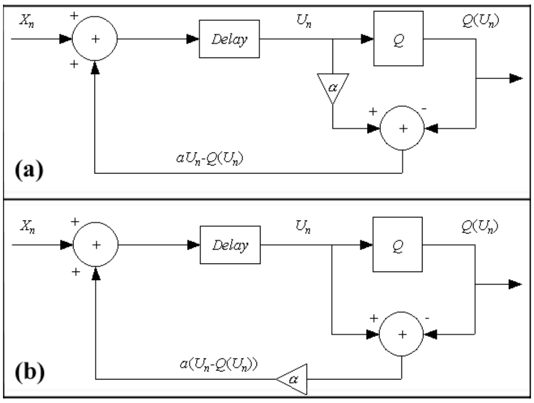

Figure 1. Block diagrams for the two systems. In (a) gain is applied to the integrator output. In (b) gain is applied to the quantizer error.

If a gain is instead added to the quantization error then the sigma delta modulator takes the form

$$U_n = X_{n-1} + \alpha(U_{n-1} - Q(U_{n-1})) \qquad (3)$$

In this work, we consider chaotic modulators where a gain term multiplies either the integrator output (1) or the error term (3). We consider whether either is an effective means of idle tone prevention. We demonstrate that for the case of gain applied to integrator output, although an implementation of a chaotic multibit modulator may lead to idle tone suppression, it may not be practical. This is because in many cases, the output of a chaotic modulator does not effectively approximate the input.

The systems

A multibit implementation of either (1) or (3) may offer increased resolution in the quantization. For an n bit first order modulator, the quantized output can assume one of $m=2^n$ states.

$$Q(u) = \begin{cases} 2(m-1)/m & \text{if} \quad um/2 \geq m-2 \\ 2(m-3)/m & m-2 > um/2 \geq m-4 \\ 2(m-5)/m & m-4 > um/2 \geq m-6 \\ \vdots & \vdots \\ -2(m-1)/m & -(m-2) > um/2 \end{cases} \qquad (4)$$

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Where we assume that quantizer input is in the range –2 to 2. The systems that will be studied are

1. The 1st order, single bit SDM with gain applied to the integrator: (1) and (2).
2. The 1st order, single bit SDM with gain applied to the error: (3) and (2).
3. The 1st order, multi bit SDM with gain applied to the integrator: (1) and (4).
4. The 1st order, multi bit SDM with gain applied to the error: (3) and (4).

Bifurcations

System 1 (Equations (1) and (2)), is perhaps the most well known and simplest form of SDM. It exhibits chaos if the gain is in the range $1 < \alpha \leq 2$. The bifurcation diagram of this system is depicted in Figure 2(a).

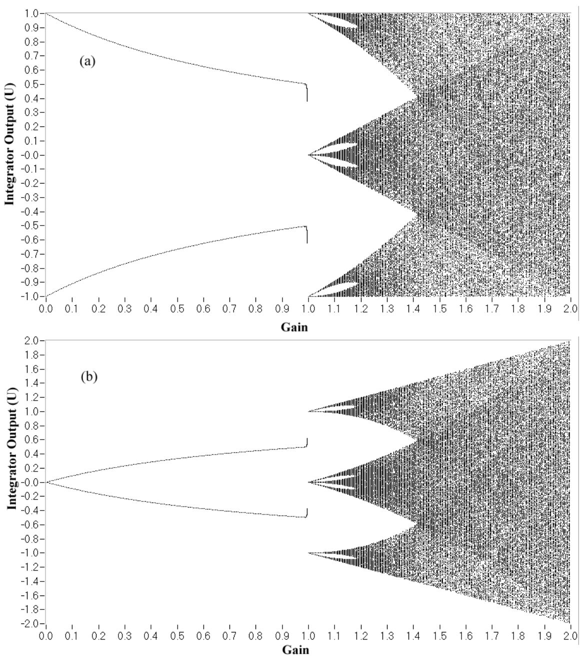

Figure 2. The bifurcation diagrams for System 1 (a) and System 2 (b) with 0 input.

System 2 has a slightly different bifurcation diagram (Figure 2b). It also exhibits chaos if the gain is in the range $1 < \alpha \leq 2$. Here, the integrator output does not immediately reach the extremes as α is increased past 1. The full range of integrator output is between –2 and 2, and for $\alpha \geq 1$, the range of output extends from $-\alpha$ to α. It may seem problematic at first, since the expected input, X, is between –1 and 1. However, as shall be seen later, as long as the average integrator output sufficiently approximates the input, then this is not a difficulty. We simply require that the input signal be bounded by ± 1, even though the quantizer can accept input bounded by ± 2.

Stability

One difficulty with operating a sigma delta modulator with greater than unity gain is that the modulator may become unstable. That is, $U_n \to \pm\infty$ as $n \to \infty$. This is illustrated in Figure 3, which depicts the size of the stable regime for constant input $0 \leq X \leq 1$ (the plot is symmetric for $-1 \leq X \leq 0$) and gain $0 \leq \alpha \leq 2$. Operating a one bit sigma delta modulator, Equation (1), in the chaotic regime becomes unworkable for any large input, since the integrator output diverges.

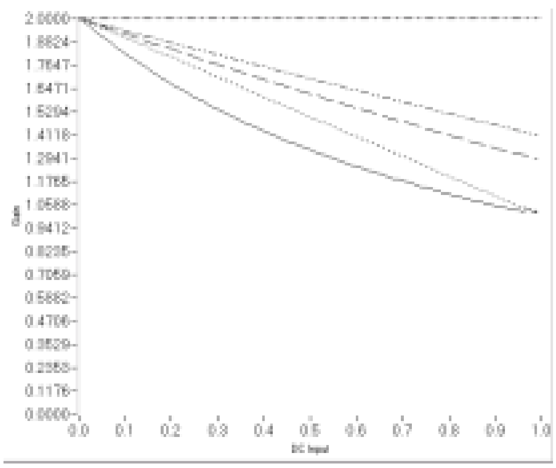

Figure 3. The stability regime for gain and constant input between 0 and 1. The solid line represents the stable regime for a 1 bit modulator with gain applied to the integrator output (System 1). The dashed line represents the stable regime for a 2 bit modulator and the dot-dot-dashed line for a 3 bit modulator (System 3). For gain applied to the error, the dotted line represents the stable regime for the 1 bit case (System 2), and the dot-dashed line represents the stable regime for the 2 bit case (System 4).

The stable regime is increased if the gain is applied to the difference between the quantizer output and the integrator output (Equation (3). For a 1 bit quantizer, the stable regime is greater than a 2 bit traditional sigma delta modulator. If we move to a 2 bit quantizer in Equation (3), then the entire domain has bounded integrator output.

Quantization Error

One requirement for SDM is that the quantizer output approximate the input signal. That is,

$$\lim_{N\to\infty}\frac{1}{N}\sum_{i=1}^{N}Q(U_i)=X \qquad (5)$$

for constant input X within a given range. With unity gain, Equation (5) holds for the single and multibit, first order sigma delta modulators. However, this is typically not true for $\alpha \neq 1$. Feely and Chua[7] showed that integrator leak, $\alpha<1$, may cause the average output of the sigma delta modulator to assume discrete values that misrepresent the input. The resulting structure of average quantized output as a function of the input is known as a devil's staircase. As shown in Figure 4, this is also the case for a traditional sigma delta modulator with $\alpha>1$(Equation (1)). In fact, for nonunity gain, the average output is approximately αX. Using a multibit modulator is not sufficient to alleviate this problem. This is a fundamental problem that is often overlooked in the literature.[7]

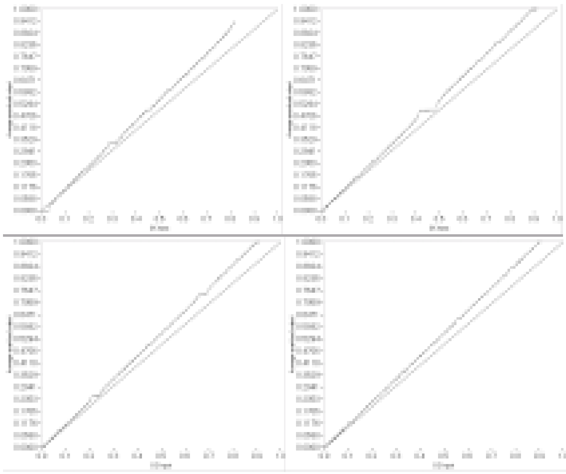

Figure 4. Clockwise from top-left. The average quantized output as a function of the input for a 1 bit, 2 bit, 3 bit, and 4 bit sigma delta modulator with gain applied to integrator output. The gain is set to 1.1. The 45 degree line represents the ideal average quantization.

The modified modulator of (3) behaves quite differently. Figure 5 shows that this modulator, although assuming discrete values, still approximates the input. In addition, a multibit implementation helps to minimize the length of the stairs in the devil's staircase structure. As the number of bits used by the quantizer is increased, the average quantized output approaches the average quantized output of an ideal sigma delta modulator.

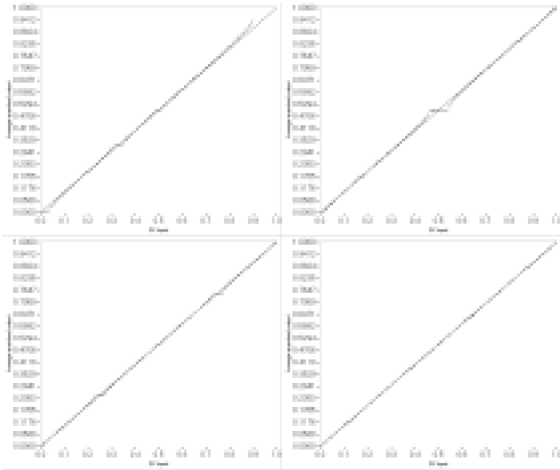

Figure 5. Clockwise from top-left. The average quantized output as a function of the input for a 1 bit, 2 bit, 3 bit, and 4 bit sigma delta modulator with gain applied to quantization error. The gain is set to 1.1. The 45 degree line represents the ideal quantization.

Symbol Sequences

On a practical level the output prior to quantization is not of primary concern. More importantly, the quantized output must accurately encode the input signal without producing idle tones. That is, tones which are not present in the analog input may appear in the digital output. For instance, a constant input of 0 with α=1 and initial condition U_0=0 will produce an output sequence of 1,-1,1,-1,1,-1… Longer period cycles will produce tones at lower frequencies which may appear audible to the listener.

One proposed method of eliminating these tones is to operate the sigma delta modulator in the chaotic regime. Although the output will still approximate the input, limit cycles might be eliminated. As an example, a constant input of 0 with α=1.5 will produce an output 1,-1,-1,1,-1,1,-1,-1,1,-1,… This is an endless pattern that never settles into a limit cycle.

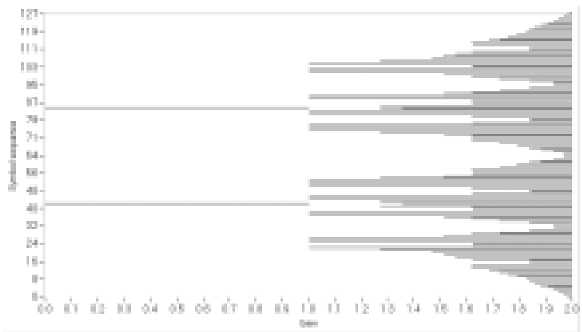

Figure 6. The permissible 7 bit sequences that can be generated using a first order, single bit sigma delta modulator.

In order to determine the range of quantized dynamics, we must investigate the symbol sequences that can be generated for various values of α. Figure 6 depicts the seven bit symbol sequences generated by a single bit sigma delta modulator with zero input (System 2). A sliding window of seven bits was applied to produce output sequences in the range 0000000 to 1111111 (0 to 127). A cyclic symbol sequence would be counted as multiple sequences, e.g., 010101… and 101010… are counted as separate allowable symbol sequences. This figure is the same for both System 1 and System 2. This demonstrates that limit cycles are more dominant with $\alpha \ll 2$ since there is a smaller range of allowable dynamics.

Power Spectra

One reason to attempt SDM in the chaotic regime is to see if it can effectively eliminate idle tones, while at the same time preserving the frequencies in the input signal. For this reason, the power spectrum is an appropriate tool.

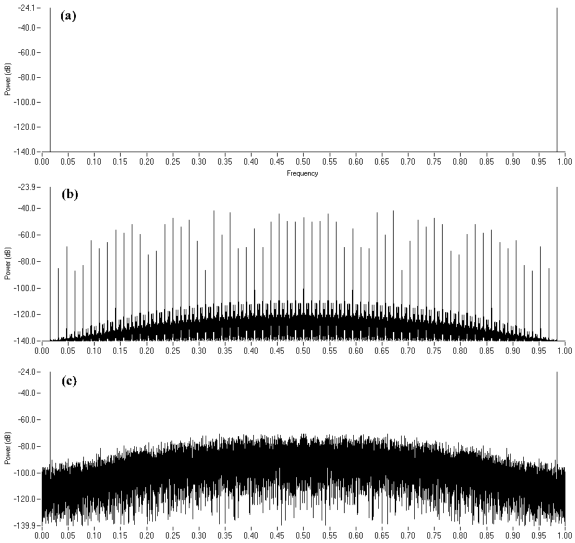

Figure 7. Power spectra for the input signal $X_n = 0.5 \cdot \sin(2\pi \cdot n/64)$. (a) is the power spectrum for the input signal, (b)for the quantized output signal with gain set to 1, and (c) for the quantized output signal with gain set to 2. The power is assumed to have a base value of 10^{-7} (-140dB).

In Figure 7, power spectra are depicted for a signal with 32 times oversampling, $X_n = 0.5 \cdot \sin(2\pi n/64)$, applied to System 4. Figure 7(a) depicts the power spectrum for the input. As expected, peaks are seen at frequencies of 1/64 and 63/64. However, for a 2 bit modulator with unity gain, the output power spectrum exhibits additional peaks at all multiples of 1/64 (Figure 7(b)). In Figure 7(c), the modulator is operated at maximum gain (Equation (3)), $\alpha = 2$. The idle tones have been replaced by chaotic fluctuations similar to broadband noise. This noise can be filtered, thus leaving only the frequencies that were apparent in the original signal.

Conclusions

A first order sigma delta modulator, where gain is applied to the integrator output, does not approximate input for $\alpha \neq 1$. If instead the gain is applied to the error in quantization, then the sigma delta modulator may achieve accurate quantization over a far greater range of input. If a multibit quantizer is used, then the modulator can be made stable over the full range of input and errors in quantization due to the Devil's staircase structure are minimized. This has the benefit that idle tones can be removed from the quantization process by operating in the chaotic regime.

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